

VLSI LABORATORY

III B.Tech. II Semester

Course Code: A226490

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COURSE OUTCOMES:

At the end of the course the student should be able

1. To learn Hardware Descriptive Language (Verilog).
2. To learn the fundamental principles of Digital System Design using HDL and FPGA.
3. To learn the fundamental principles of VLSI circuit design in digital domain
4. To analyze various combinational and sequential circuits using Verilog HDL
5. To provide hands on design experience with EDA platforms.

Perform any 10 Experiments:

1. Verification of Logic Gates
2. Verification of Demorgan's Law
3. Design of 8 to 1 multiplexer
4. Design of 1 to 8 Demultiplexer
5. Design of 2 to 4 Encoder
6. Design of 4-bit comparator
7. Design of 4 bit binary to gray converter
8. Design of full adder using 3 modeling styles
9. Design of flip flops SR, D, JK, and T
10. Design Ripple Counter
11. Design Modulo Counter
12. Design Shift Register
13. Design Inverter using PMOS / NMOS
14. Design of full adder using decoder and multiplexer
15. Design System using finite state Machine