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**VIDYA JYOTHI INSTITUTE OF TECHNOLOGY**

*AZIZNAGAR GATE, CHILUKUR ROAD, HYDERABAD  
500075*

(AN AUTONOMOUS INSTITUTION)

**ONE DAY HANDS-ON-TRAINING  
ON  
ADVANCED DIGITAL DESIGN USING SIMULINK**

on 29<sup>nd</sup> Feb 2020

**REGISTRATION FORM**

NAME OF THE PARTICIPANT: .....

DEPARTMENT: .....

INSTITUTION: .....

ADDRESS: .....

.....

CONTACT NO. (MOBILE): .....

E-MAIL: .....

FEE DETAILS: .....

AMOUNT: ..... D.D NO: .....

BANK & BRANCH: .....

SIGN. OF THE APPLICANT: .....

AMOUNT RECEIVED: .....

SIGNATURE OF APPLICANT

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**ORGANIZED BY**

**DEPARTMENT OF  
ELECTRONICS & COMMUNICATION  
ENGINEERING  
&  
IEEE STUDENT CHAPTER**

## ABOUT THE COLLEGE

Vidya Jyothi Institute of Technology (VJIT) was established in 1999. Situated in the backdrop of Osmansagar (Gandipet) lake in the serene surroundings of Chilkur Balaji Temple, VJIT has a sprawling and lush green campus with architecturally splendid buildings in an area of 12 acres.

The college has got a rich library of books, a state-of-art internet lab, and modern labs for each Department, a central workshop, sports and games facilities. The college is accredited by NAAC & NBA of AICTE.

The college prides on the fact that it has a very senior and highly accomplished faculty- one of the best in the region. VJIT is rated as one of the best engineering colleges in the region.

## ABOUT THE DEPARTMENT

The department of ECE is a major strength of the institute. The department has an excellent group of faculty having teaching industry and research experience.

The department of ECE offers P.G/U.G Programs M.Tech/B.Tech with an intake of M.Tech 36/ B.Tech 240 seats. The department has well equipped laboratories. We nurture the young talent available in the country and transform them into enterprising technologists so that they contribute immensely to the technological development and prosperity of the country and provide dynamic leadership to others.

The department is also equipped with exclusive research labs like NI Labview center of excellence, ARM University Program & Cypress PSOC Semiconductors Laboratory.

## ABOUT THE WORKSHOP

All digital systems are founded on logic design. Logic design transforms algorithms and processes conceived by people into computing machines. A grasp of digital logic is crucial to the understanding of other basic elements of digital systems, including microprocessors. Design Engineer need to translate the system specification into circuit description, this can be achieved using schematic capture tools like Proteus or by describing the design using textual form much like software program. Textual descriptions of digital hardware can be written in programming language such as C, or in a hardware description language (HDL).

## SCOPE

The objective of this one day training is mainly targeting the students who are interested to work in the field of digital design domain. The training will provide an opportunity to understand the concepts of creation of models in Simulink, usage of IPs and their implementation in IP integrator.

## TOPICS TO BE FOCUSED

- Creating models in Simulink.
- Converting designed models into HDL code.
- Creating an IP using Vivado design tool.
- Implementation and synthesis of IPs in IP integrator.

## RESOURCE PERSON

**Mr. G. Surender,**  
**Senior Hardware Design Engineer,**  
**Reliance Jio Infocomm Limited,**  
**Mumbai.**

## ELIGIBILITY

The programme is opened to the students under Electronics and Communication domain and research scholars and technocrats those who are working in industries.

## REGISTRATION

A filled in form of application in the prescribed format duly signed by appropriate authorities should reach us by post or e-mail.

## SELECTION

The selection is purely on first-cum-first serve basis as the number of participants is limited to a maximum of 40 only. The participants are requested to inform their willingness on or before 22<sup>th</sup> Feb 2020 to make necessary arrangement.

## FOR FURTHER DETAILS PLEASE CONTACT

## IEEE STUDENT COUNSELOR

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